Claims

1. A semiconductor integrated circuit comprising:

an input circuit for taking in signals; and

an output circuit for outputting signals,

wherein the input circuit is so set that an input impedance during input signal transition is lower than an input impedance on other occasions than input signal transition, and

wherein the output circuit is so set that a driving force during a second half of signal transition is lower than a driving force during a first half of transition.

2. The semiconductor integrated circuit according to Claim 1,

wherein the input circuit and the output circuit are connected in common to a pad that enables inputting/outputting of signals.

3. A semiconductor integrated circuit comprising:

an input pad; and

an input circuit for taking in external signals through the input pad,

wherein the input circuit includes a dynamic terminator resistor circuit that can be adjusted so that an input impedance during input signal transition is lower than an input impedance on other occasions than input signal transition.

4. The semiconductor integrated circuit according to Claim 3,

wherein the dynamic terminator resistor circuit comprises:

a first logic circuit for inverting the logic of a signal transmitted through the input pad;

a second logic circuit for inverting the logic of the output signal of the first logic circuit; and

a resister that can connect the input terminal of the first logic circuit with the output terminal of the second logic circuit.

5. The semiconductor integrated circuit according to Claim 3,

wherein the dynamic terminator resistor circuit comprises:

a first logic circuit for inverting the logic of a signal transmitted through the input pad;

a second logic circuit for inverting the logic of the output signal of the first logic circuit;

a resister that can connect the input terminal of the first logic circuit with the output terminal of the second logic circuit; and

a third logic circuit for transmitting the output signal of the first logic circuit to an internal circuit.

6. The semiconductor integrated circuit according to Claim 4 or Claim 5, including:

a switch circuit capable of controlling the involvement of the resister with circuit operation.

7. The semiconductor integrated circuit according to Claim 4 or Claim 5,

wherein the dynamic terminator resistor circuit comprises:

a first logic circuit for inverting the logic of a signal transmitted through the input pad;

a second logic circuit for inverting the logic of the output signal of the first logic circuit;

a plurality of resisters that can connect the input terminal of the first logic circuit with the output terminal of the second logic circuit; and

a switch circuit for selectively getting a plurality of the resisters involved with circuit operation.

8. A semiconductor integrated circuit comprising:

an internal circuit; and

an output circuit that can externally output the output signal of the internal circuit,

wherein the output circuit comprises:

a first output circuit that can drive an external load based on the output signal of the internal circuit during a first half of transition of a signal to be outputted; and

a second output circuit whose driving force is set

lower than that of the first output circuit and which can drive the external load.

9. The semiconductor integrated circuit according to Claim 8, including:

a level monitor circuit for selectively getting the first output control circuit or the second output circuit involved with circuit operation according to the voltage level of the external load.

10. The semiconductor integrated circuit according to Claim 8,

wherein the second output circuit includes a series connection circuit of an n-channel transistor disposed on a higher-potential power supply side and a p-channel transistor disposed on a lower-potential power supply side, and a series connection node between the n-channel transistor and the p-channel transistor is coupled to the output node of the first output circuit.

11. A semiconductor integrated circuit comprising:

an input portion so set that an input impedance during input signal transition is lower than an input impedance on other occasions than input signal transition; and

an output portion so set that a driving force during a second half of signal transition is lower than a driving force during a first half of transition,

wherein the output portion comprises:

a first output circuit that can drive an external load based on the output signal of the internal circuit during the first half of transition of a signal to be outputted; and

a second output circuit whose driving force is set lower than that of the first output circuit and which can drive the external load,

wherein the second output circuit includes a series connection circuit of an n-channel transistor disposed on a higher-potential power supply side and a p-channel transistor disposed on a lower-potential power supply side, and

wherein a series connection node between the n-channel transistor and the p-channel transistor is connected in common to the input/output pad together with the output node of the first output circuit, and the series connection circuit is also used as part of the input portion.